Unit -> 1 Diode Circuits

Subject -> Analog Circuits

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Paper code -> BT 402

Lecture 5 -> Fet biasing

$$V_{GS2} = 5 - 0 = 5\ \text{V}$$

T_2 is nonconducting, OFF (its VT is negative), draws only leakage current, offers high resistance (R_2)

$$V_{GS1} = 5\ \text{V} > V_T$$

T_1 is conducting, ON; offers very low resistance (R_1). The circuit equivalent in this state is drawn in Fig. 16.20(b).

Output

$$V_o \approx 0 \Rightarrow 0\text{-state}$$

It can be seen from the circuits of Fig. 16.20(b) that

$$V_o = \frac{R_1}{R_1 + R_2} V_{SS} \approx 0\ \text{V}$$

2. Input

$$V_i = 0\ \text{V} \Rightarrow 0\text{-state}$$

$$V_{GS2} = -5\ \text{V},\ T_2 \text{ conducting (low resistance)}$$

$$V_{GS1} = 0\ \text{V};\ T_1 \text{ nonconducting (high resistance)}$$

Output

$$V_o \approx 5\ \text{V} \Rightarrow 1\text{-state}$$

We thus see that the circuit acts as an inverter; 1-state input produces 0-state output and 0-state inpu produces 1-state output.

It is observed in this circuit that only one transistor is turned on in any of the output states. As th transistors are series connected, no current is drawn from the battery source in either of the two state Current is drawn from the battery only during state transition (either way). CMOS circuits, therefore, dra extremely low power from the battery source and so their energy consumption is very small. This is t major attraction why CMOS is used in digital applications.

16.6 FET BIASING

We shall consider only voltage-divider biasing as this is most commonly adopted. By examining the drain characteristics of the device, a Q-point is selected in the middle of the saturation region, which fixes V_{GSQ} and I_{DQ}. The biasing circuit resistors are to be selected for the device under dc conditions to operate at the Q-point.

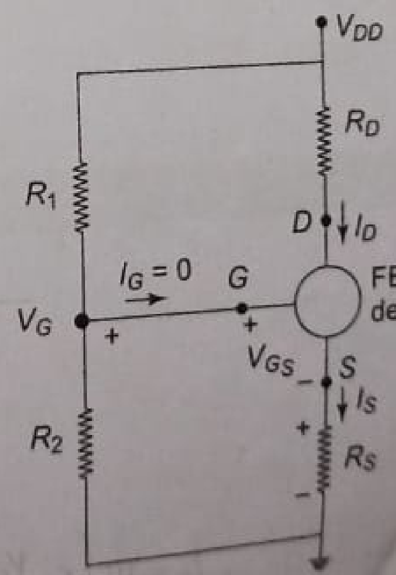

Fig. 16.21

16.6.1 Voltage Divider Biasing

The circuit is drawn in Fig. 16.21. It is the same for any FET.

As per voltage divider

$$V_G = \left(\frac{R_2}{R_1 + R_2}\right) V_{DD} \tag{16.8}$$

Then

$$V_{GS} = V_G - I_D R_S,\ I_S = I_D \tag{16.9}$$

$I_D R_S$ provides stabilising negative voltage feedback.

Device transfer characteristic,

$$I_D = f(V_{GS})|_{\text{Device Parameters}}; \text{ nonlinear} \tag{16.10}$$

As V_{GSQ} has been chosen, the choice of R_S and simultaneous solution of Eqs (16.8) and (16.9) yields I_{DQ}.

KVL for *DS* load yields

$$V_{DSQ} = V_{DQ} - I_D(R_S + R_D),\ R_D \text{ has to be selected} \tag{16.11}$$

Biasing analysis/design is then complete.

Simultaneous Solution of Eqs. (16.9) and (16.10)

(i) Equation (16.10) is the transfer characteristic of FET (nonlinear function of V_{GS}). Equation (16.9) is a straight line, whose intersection with the transfer characteristic yields I_{DQ} and V_{GSQ}.

or

(ii) Substituting I_D from Eq. (16.9) in Eq. (16.10) leads to a quadratic equation in V_{GS} yielding two solutions from which the appropriate one is to be chosen.

JFET

Refer Fig. 16.21.

JFET: $I_{DSS} = 10$ mA, $V_P = -6$ V

Circuit: $R_1 = 2.2$ MΩ, $R_2 = 280$ kΩ, $V_{DD} = 16$ V

$R_D = 2$ kΩ, $R_S = 1.5$ kΩ

To determine at *Q*-point

V_{GS}, I_D, V_{DS}, V_{DG}

Plot the transfer characteristic (Fig. 16.22).

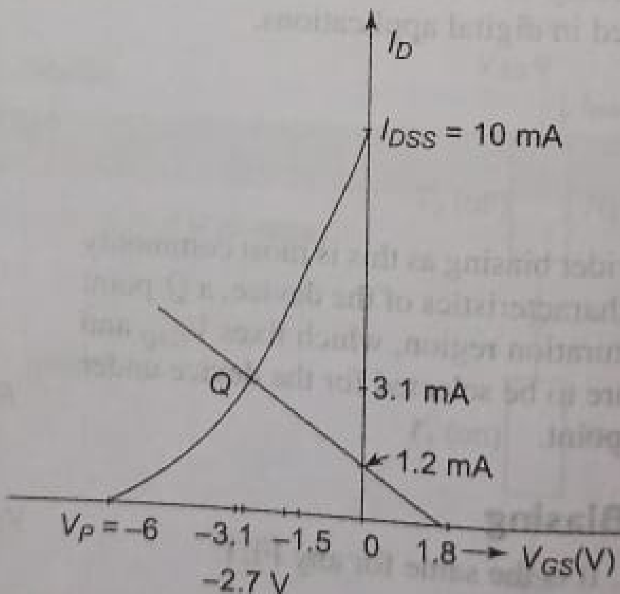

Fig. 16.22 *Transfer characteristic*

$$I_D = 10\left(1 - \frac{V_{GS}}{V_P}\right)^2 \tag{16.12}$$

$$V_{GS} = -3\text{ V},\ \frac{V_{GS}}{V_P} = \frac{1}{2},\ I_D = 2.5\text{ mA}$$

$$V_{GS} = 1.5\text{ V}, \frac{V_{GS}}{V_P} = \frac{1}{4}, I_D = 5.265\text{ mA}$$

Plot Eq. (16.7).

$$V_G = \frac{280}{2.2 \times 10^3 + 280} \times 16 = 1.8\text{ V}$$

$$V_{GS} = 1.8 - 1.5\, I_D \tag{16.13}$$

$$I_D = 0, V_{GS} = 1.8\text{ V}$$

$$V_{GS} = 0, I_D = \frac{1.8}{1.5} = 1.2\text{ mA}$$

At intersection, Q-point $\Rightarrow V_{GS} = -2.7\text{ V}\ I_D = 3.1\text{ mA}$

$$V_{DS} = 16 - (2 + 1.5) \times 3.1 = 5.15\text{ V}$$

Analytic Approach

From Eq. (16.13),

$$I_D = \frac{2.8 - V_{GS}}{1.5} = 1.2 - 0.67\, V_{GS} \tag{16.14}$$

Substituting I_D in Eq. (16.13),

$$1.2 - 0.67\, V_{GS} = 10\left(1 - \frac{V_{GS}}{-6}\right)^2$$

Let $V_{GS} = x$

$$1.2 - 0.67x = 10\left(\frac{6+x}{6}\right)^2 = \frac{10}{36}(6+x)^2$$

$$4.32 - 2.41x = x^2 + 12x + 36$$

$$x^2 + 14.41x + 31.68$$

$x = -2.7, -11.7$ (rejected as more negative than V_P)

Then $V_{GS} = -2.7\text{ V}$

The same result as obtained by the graphical solution.

DMOSFET

Refer Fig. 16.21.

DMOSFET parameters

$$I_{DSS} = 8\text{ mA}, V_p = -4$$

Circuit data

$$V_{DD} = 16\text{ V}$$

$$R_1 = 100\text{ M}\Omega, R_2 = 10\text{ M}\Omega,$$

$$R_D = 1.6\text{ k}\Omega, R_S = 700\ \Omega$$

To determine

$$I_{DQ}, V_{GSQ}, V_{DSQ}$$

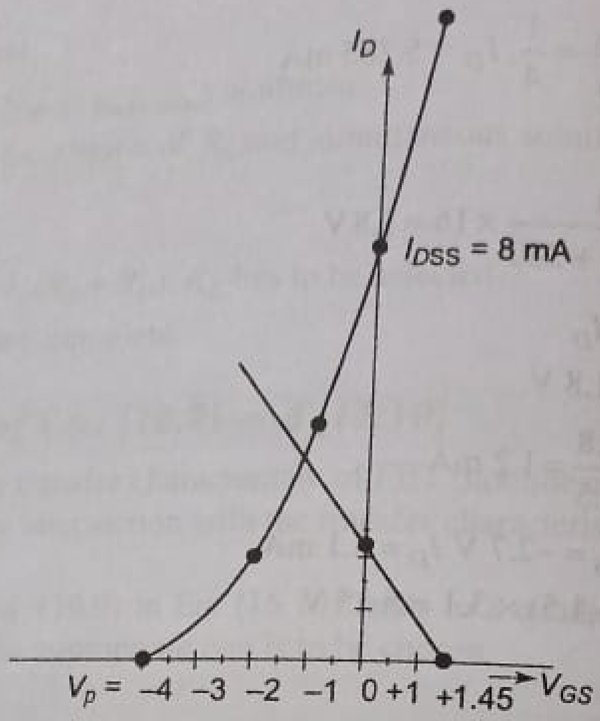

Fig. 16.23 *Transfer characteristic*

Plotting transfer characteristic (Fig. 16.23),

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$V_{GS} = -2\text{ V}; I_D = 8\left(1 - \frac{1}{2}\right)^2 - 2\text{ mA}$$

$$V_{GS} = -1\text{ V}, I_D = 8\left(1 - \frac{1}{4}\right)^2 = 4.5\text{ mA}$$

$$V_{GS} = +1\text{ V}, I_D = 8\left(1 - \frac{1}{4}\right)^2 = 12.5\text{ mA}$$

Plotting Eq. (16.8),

$$V_G = \frac{10}{100+10} \times 16 = 1.45\text{ V}$$

$$V_{GS} = V_G - 0.7\, I_D$$

$$I_D = 0 \qquad V_{GS} = V_G = 1.45\text{ V}$$

$$V_{GS} = 0 \qquad I_D = \frac{1.45}{0.7} = 2.07\text{ mA}$$

At intersection, Q-point

$$I_{DQ} = 3.8\text{ mA}, V_{GSQ} = -1.2\text{ V}$$

From Eq. (16.10),

$$V_{DSQ} = 16 - (1.6 + 0.7) \times 3.8 = 7.26\text{ V}$$

Refer Fig. 16.21.

EMOSFET parameters

$$V_T = 4\text{ V}, V_{GS(on)} = 8\text{ V}, I_{D(on)} = 2.5\text{ mA}$$

Biasing circuit

$$V_{DD} = 35\text{ V}, R_1 = 20\text{ M}\Omega, R_2 = 16\text{ M}\Omega$$
$$R_D = 2.5\text{ k}\Omega, R_S = 0.75\text{ k}\Omega$$

To determine: At Q-point

$$I_{DQ}, V_{GSQ}, V_{DS}$$

Plot transfer characteristic (Fig. 16.24).

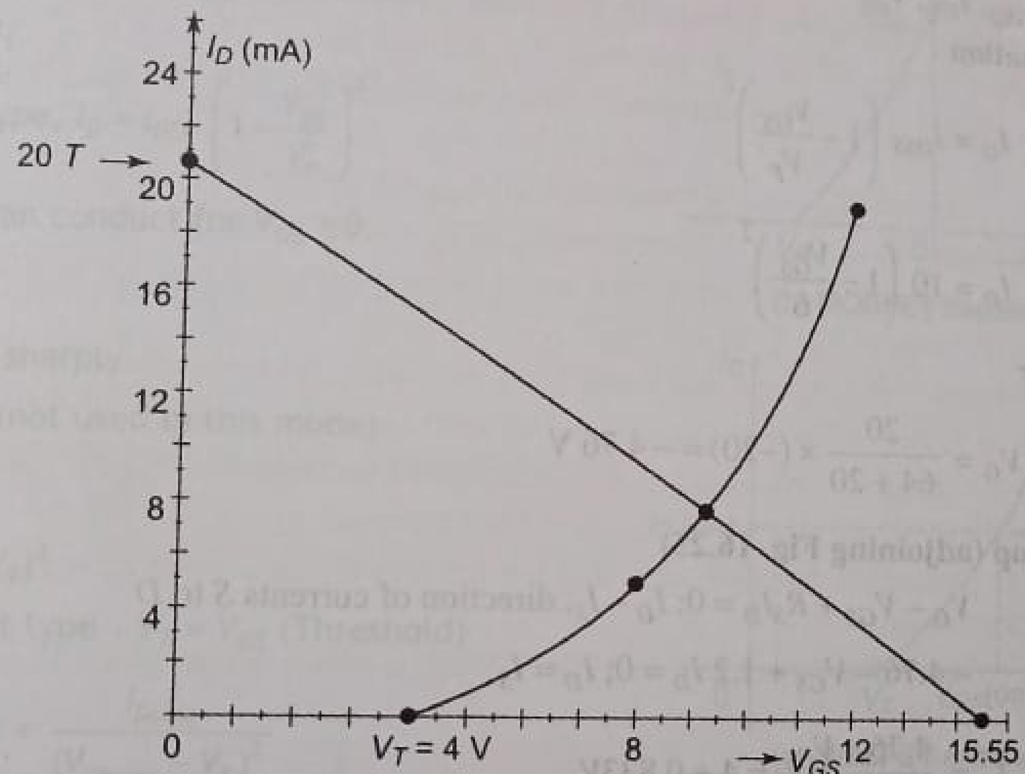

Fig. 16.24

$$k = \frac{2.5}{(8-4)^2} = 0.156\text{ mA/V}^2$$
$$I_D = 0.156\,(V_{DS} - 4)^2$$
$$V_{GS} = 8\text{ V}, I_D = 0.156 \times 16\ 2.5\text{ mA}$$
$$V_{GS} = 12\text{ V}, I_D = 0.156 \times 64 = 10\text{ mA}$$

Plot Eq. (16.8).

$$V_G = \frac{16}{20+16} \times 35 = 15.55\text{ V}$$
$$V_{GS} = 15.55 - 0.75\,I_D$$
$$V_{GS} = 0, I_D = 20.7\text{ mA}$$
$$I_D = 0,\ V_{GS} = 15.55$$

At Q-point,

$$V_{GSQ} = 9.2\text{ V}, I_{DQ} = 8.4\text{ mA}$$

From Eq. (16.11),

$$V_{DS} = 35 - (2.5 + 0.7) \times 8.4 = 8.12 \text{ V}$$

p-channel JFET

Refer Fig. 16.21 directions of I_D and I_S reverse, V_{DD} is negative, JFET parameters $I_{DSS} = 10$ mA, $V_P = 6$ V (positive).

Biasing circuit

$$V_{DD} = -20 \text{ V}, R_1 = 64 \text{ k}\Omega, R_2 = 20 \text{ k}\Omega$$

$$R_D = 2 \text{ k}\Omega. Rs = 1.2 \text{ k}\Omega$$

To determine at *Q*-point

$$V_{GSQ}, I_{DQ}, V_{DS}$$

Shockley's equation

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$I_D = 10\left(1 - \frac{V_{GS}}{6}\right)^2$$

Voltage divider

$$V_G = \frac{20}{64+20} \times (-20) = -4.76 \text{ V}$$

KVL for *GS* loop (adjoining Fig. 16.25)

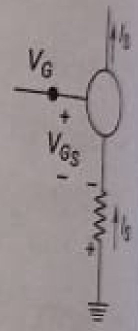

Fig. 16.25

$$V_G - V_{GS} + R_S I_D = 0; I_D - I_S; \text{ direction of currents } S \text{ to } D$$

$$-4.76 - V_{GS} + 1.2\, I_D = 0; I_D = I_S$$

or $$I_D = \frac{4.76 + V_{GS}}{1.2} = 4 + 0.833 V_{GS} \quad (16.15)$$

Let $V_{GS} = x,$

Substituting I_D in Eq (16.15),

$$4 + 0.833x = \frac{10}{36}(6-x)^2$$

$$14.4 + 3x = 36 - 12x + x^2$$

$$x^2 - 15x + 21.6 = 0 \Rightarrow x = 1.6 \text{ V}, 13.476 \text{ V (rejected)}$$

Then,

$$V_{GSQ} = 1.6 \text{ V}$$

$$I_{DQ} = 10\left(1 - \frac{1.6}{8}\right)^2 = 5.38 \text{ mA}$$

KVL *DS* loop,

$$-20 - (2 + 1.2) \times 5.38 - V_{DS} = 0$$

or $$V_{DS} = -2.78 \text{ V}$$